Table of Contents

1 Calling Conventions 1

1.1 Introduction 1
1.2 Processor Background 1
1.3 Calling Mechanism 2
1.4 Register Usage 2
1.5 Parameter Passing 2
1.6 User-Provided Routines 2
1.7 Leaf Procedures 2

2 Memory Model 3

2.1 Introduction 3
2.2 Flat Memory Model 3

3 Interrupt Processing 5

3.1 Introduction 5
3.2 Vectoring of Interrupt Handler 5
3.3 Interrupt Record 6
3.4 Interrupt Levels 6
3.5 Disabling of Interrupts by RTEMS 7
3.6 Register Cache Flushing 7
3.7 Interrupt Stack 8

4 Default Fatal Error Processing 9

4.1 Introduction 9
4.2 Default Fatal Error Handler Operations 9

5 Board Support Packages 11

5.1 Introduction 11
5.2 System Reset 11
5.3 Processor Initialization 11

6 Processor Dependent Information Table 13

6.1 Introduction 13

6.2 CPU Dependent Information Table 13

7 Memory Requirements 17

7.1 Introduction 17
7.2 Data Space Requirements 17
7.3 Minimum and Maximum Code Space Requirements 17
7.4 RTEMS Code Space Worksheet 18
7.5 RTEMS RAM Workspace Worksheet 18

8 Timing Specification 21

8.1 Introduction 21
8.2 Philosophy 21
8.2.1 Determinancy 22
8.2.2 Interrupt Latency 23
8.2.3 Context Switch Time 24
8.2.4 Directive Times 24
8.3 Methodology 25
8.3.1 Software Platform 25
8.3.2 Hardware Platform 25
8.3.3 What is measured? 25
8.3.4 What is not measured? 26
8.3.5 Terminology 26

9 Timing Data 29

9.1 Introduction 29
9.2 Hardware Platform 29
9.3 Interrupt Latency 30
9.4 Context Switch 30
9.5 Directive Times 30
9.6 Task Manager 31
9.7 Interrupt Manager 32
9.8 Clock Manager 32
9.9 Timer Manager 33
9.10 Semaphore Manager 34
9.11 Message Manager 35

9.12 Event Manager 36
9.13 Signal Manager 36
9.14 Partition Manager 36
9.15 Region Manager 37
9.16 Dual-Ported Memory Manager 37
9.17 I/O Manager 37
9.18 Rate Monotonic Manager 38